
Application Note

MEASURING THE PERFORMANCE OF POWER SUPPLY REJECTION FEEDBACK AS USED IN CS44800/44600 DIGITAL CLASS-D PWM AMPLIFIERS

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1. Introduction

Most currently available digital Class-D amplifiers are termed “open-loop” systems since no mechanisms have been developed to provide real-time feedback to reject unwanted tones (ripple) generated by the power supply, or the noise coupled onto the power rail due to ripple currents flowing through large decoupling capacitors. Since the high sides of the power MOSFETs are connected directly to the power supply rail, all tones and associated harmonics generated on the power supply rail are coupled onto the output of the audio amplifier channel.

Costly detection and feedback circuitry must be added to the power supply to account for output voltage variations due to load current fluctuations. In addition, the output voltage rail must be designed to remain stable as the input AC voltage deviates from the nominal 120 V. Any drift from the nominal design point will be directly reflected in the output DC voltage rail causing audible volume changes during playback. To overcome these inherent limitations of conventional “open-loop” Class-D amplifiers, tightly regulated power supplies are commonly employed.

Utilizing the integrated PSR Feedback, it is shown that a digital Class-D PWM amplifier implemented with the CS44800/44600 PWM Controller is now an effective power supply “closed-loop” system by employing real-time feedback of the voltage rail. Real-time voltage feedback now enables this digital Class-D PWM amplifier to operate with any type of power supply, with any measure of output regulation. To demonstrate the rejection/compensation for the above-mentioned deficiencies, a procedure is described below that uses the CDB44800 development board to emulate a system which contains a large amount of tones and harmonics on the power supply rail.

Power supply costs can now be reduced and other power supply technologies used. “Open-loop” digital Class-D PWM amplifiers prohibit the use of traditional low-cost, dependable, low-EMI-radiated-noise, unregulated, linear power supplies. Published application notes for current Class-D amplifier systems on the market recommend the use of switch mode power supplies with very low output voltage ripple and tight regulation for both load and line variations, in conjunction with large, expensive, low-ESR electrolytic capacitors. The CS44800/44600 PSR circuitry eliminates these dependencies and allows for inexpensive power supply alternatives to be used.

2. PSR Feedback Measurement Procedure

2.1 Power Supply Rejection Performance Test

The test platform used for the performance measurement plots below consists of the CDB44800 (half-bridge channels), with $V_{power} = +40\text{ V}$, and a resistive load of $6\ \Omega$. Channel A of the input audio stream was set to channel 3 on the development board and channel B was set to channel 8.

- 1) Use an unregulated power supply if available. The PSR rejection performance can be seen using any type of power supply, however the actual amount of rejection due to PSR feedback will be more visible with a lightly regulated power supply than with a highly regulated power supply. PSR calibration should be done before any of the channels are enabled so an accurate representation of the nominal voltage rail can be captured. See the CS44800/600 datasheet for the PSR calibration routine.
- 2) Set up the board under test for 2-channel operation with $6\text{-}\Omega$ resistive loads and execute the appropriate script file such that amplified audio is playing from the board and PSR is calibrated. Verify that PSR Feedback is disabled (CS44800/44600 bit 5 in register 34h set to 0b). The two channels being used should be in separate power packages, such as channel 3 and channel 8 on the CDB44800, to minimize the effects of switching noise.
- 3) Using a digital audio source (such as an Audio Precision), set channel A to be a -1-dBFS , 1-kHz sine wave and set channel B to be a 0-dB , 60-Hz sine wave. Channel B is being used to emulate the harmonics generated by an inexpensive, poorly regulated power supply. The 60-Hz switching output of channel B will generate a corresponding ripple voltage on the rail, which will couple into the channel under test, in this case channel A.
- 4) With only the channel A PWM output turned on, use an analog analyzer (such as an Audio Precision) and take an FFT of amplitude versus frequency for channel A. The 1-kHz tone should be present with an amplitude of -1 dBFS . Figure 1 shows the results with only channel A enabled as a baseline.

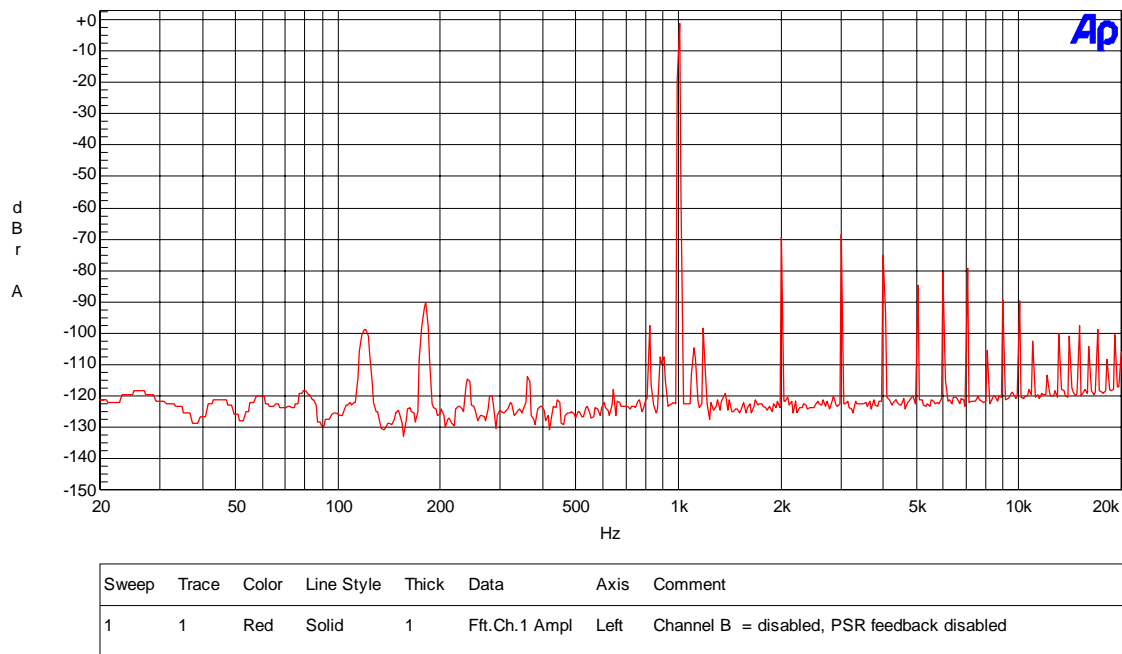


Figure 1. FFT Amplitude vs. Frequency,
Channel A = 1 kHz , -1 dBFS , Channel B = disabled, PSR feedback disabled

- 5) Turn on the channel B PWM output and take an FFT of amplitude versus frequency for channel A. The 1-kHz tone should be present with an amplitude of -1 dBFS (with modulated side tones) along with a 60-Hz tone and associated harmonics. Figure 2 shows the FFT of channel A with both channel A and channel B PWM outputs enabled. The original 1-kHz tone is shown at -1 dBFS, with the coupled 60-Hz tone from channel B shown at -50 dBFS. The full scale, 60 Hz tone being played back on channel B's MOSFET devices causes an associated 60-Hz ripple current on the power voltage rail. This ripple current, along with the capacitor's equivalent series resistance (ESR), causes the discrete tones on the power supply rail. Notice the 2nd, 3rd, 4th, 5th, etc. harmonics at 120 Hz, 180 Hz, 240 Hz, 300 Hz, etc. due to the system non-linearities. Because all of these tones are being modulated onto channel A's audio output by the power MOSFETs switching at a 384-kHz rate, these discrete tones will also be modulated onto the 1-kHz tone being played back (see tones grouped around 1 kHz). These modulated tones appear as symmetrical, equidistant tones on each side of the 1-kHz tone. The amplitude and frequency of each modulated tone is easily calculated using standard FM modulation formulas.

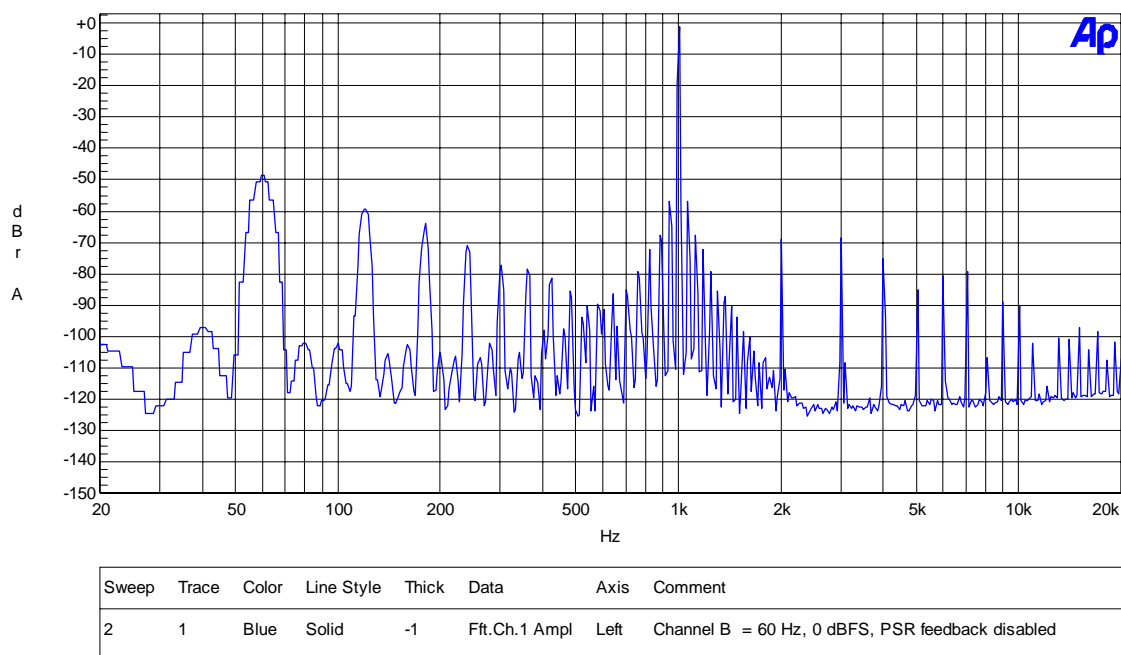


Figure 2. FFT Amplitude vs. Frequency,
 Channel A = 1 kHz, -1 dBFS, Channel B = 60 Hz, 0 dBFS, PSR feedback disabled

- 6) Enable PSR Feedback (CS44800/44600 bit 5 in register 34h set to 1b). Take an FFT of amplitude versus frequency on the output of channel A. The 1-kHz tone should be present with an amplitude of -1 dBFS, however the 60-Hz tone and the modulated side tones will be greatly diminished in amplitude. Figure 3 shows the results of having both channels on and PSR feedback enabled.

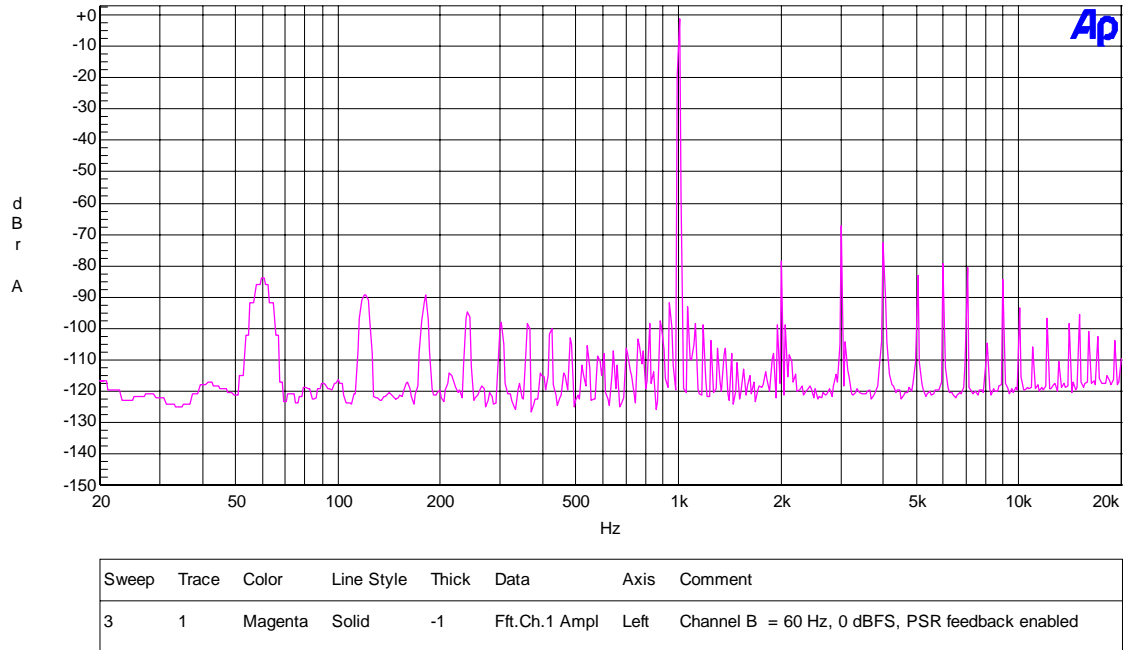


Figure 3. FFT Amplitude vs. Frequency,
 Channel A = 1 kHz, -1 dBFS, Channel B = 60 Hz, 0 dBFS, PSR feedback enabled

Figure 4 shows the results from Figure 2 and Figure 3 as an overlay.

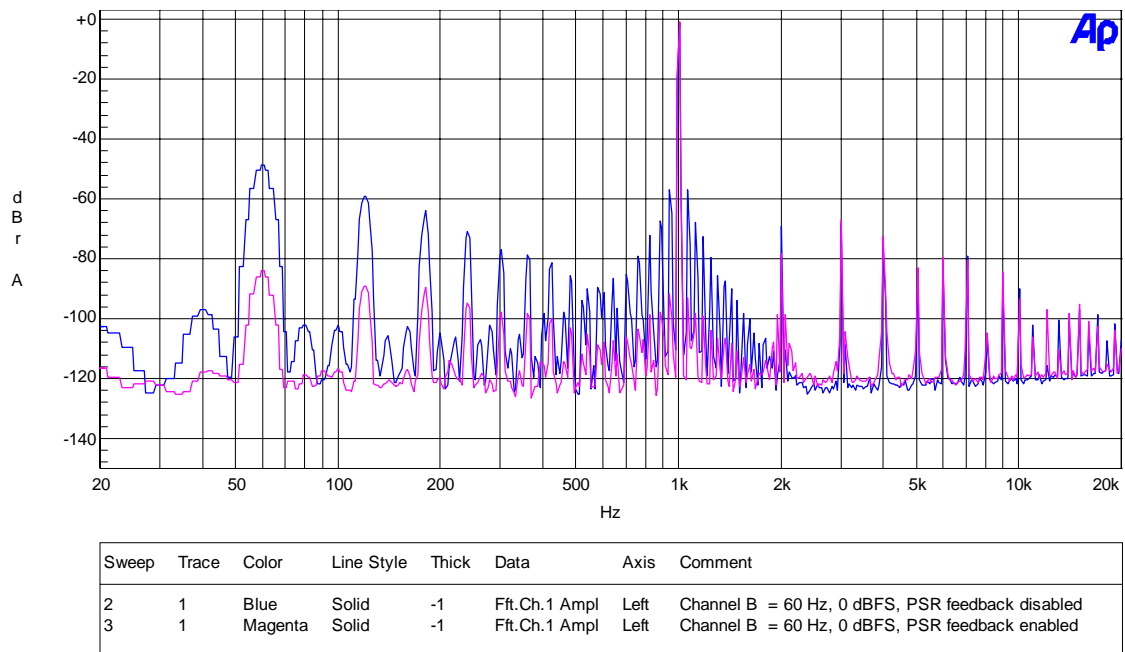


Figure 4. FFT Amplitude vs. Frequency,
 Figure 2 & Figure 3 overlay

- 7) To show the effect of this noise modulation on low-level audio signals, set the amplitude of the 1kHz tone on channel A to -60 dBFS. Channel B remains at 60 Hz, 0 dBfs signal. Figure 5 shows the same tests as above. The blue trace is the FFT of channel A's output with PSR turned off. The magenta trace represents channel A's output with PSR feedback enabled.

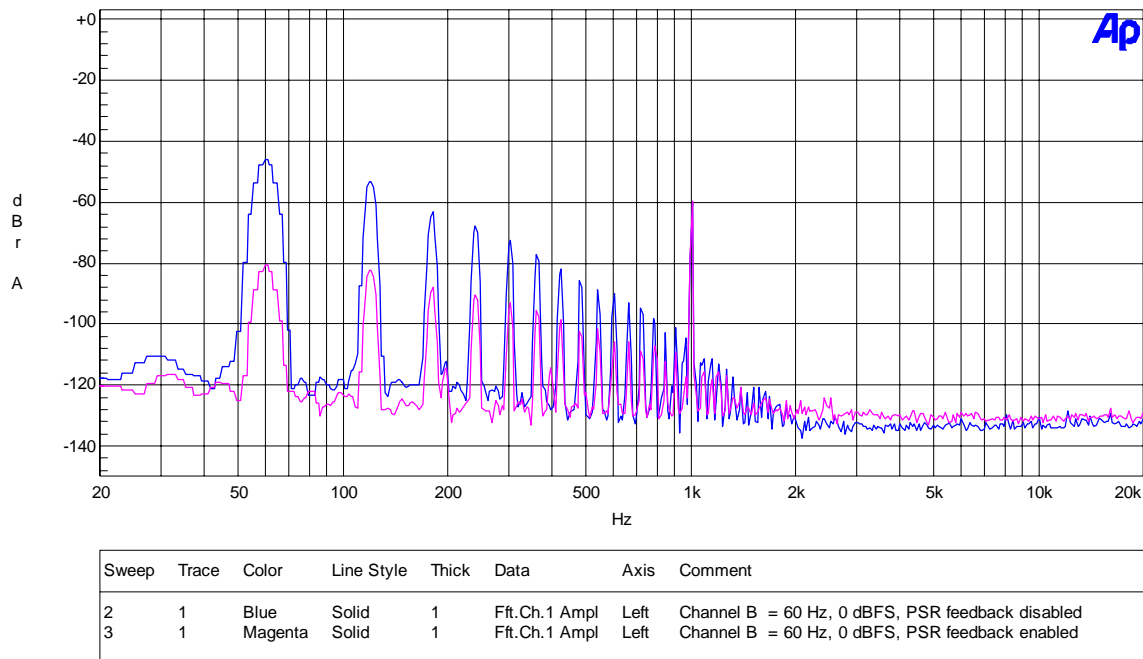


Figure 5. FFT Amplitude vs. Frequency,
 Channel A = 1 kHz, -60 dBFS, Channel B = 60 Hz, 0 dBFS, PSR feedback enabled/disabled

2.2 PSR Feedback Performance Versus Frequency

The following graph in Figure 6 shows the amount of rejection that PSR Feedback will provide versus the frequency of the power supply noise (typically in the low-frequency range). The frequency on channel B, which induces the ripple voltage on the channel under test (channel A), is varied from 20 Hz to 20 kHz. The plot represents the amplitude of the coupled noise from the power supply rail onto channel A vs. the frequency of the coupled noise.

Zero data is sent to channel A, which is equivalent to muting the amplifier output (not MUTE50/50). Channel A's output is not turned off, but rather switches at a modulated nominal 50% duty cycle at a 384-kHz rate. The red trace in the graph represents the amount of ripple voltage which is coupled onto channel A's output from the 0-dBFS signal being played back on channel B. Since the output of channel A continues to switch, modulation with another channel will still occur. The natural decay in the amount of ripple voltage present on channel A's output at higher frequencies is due to the frequency-dependant reactance of the large, bulk decoupling electrolytic capacitor.

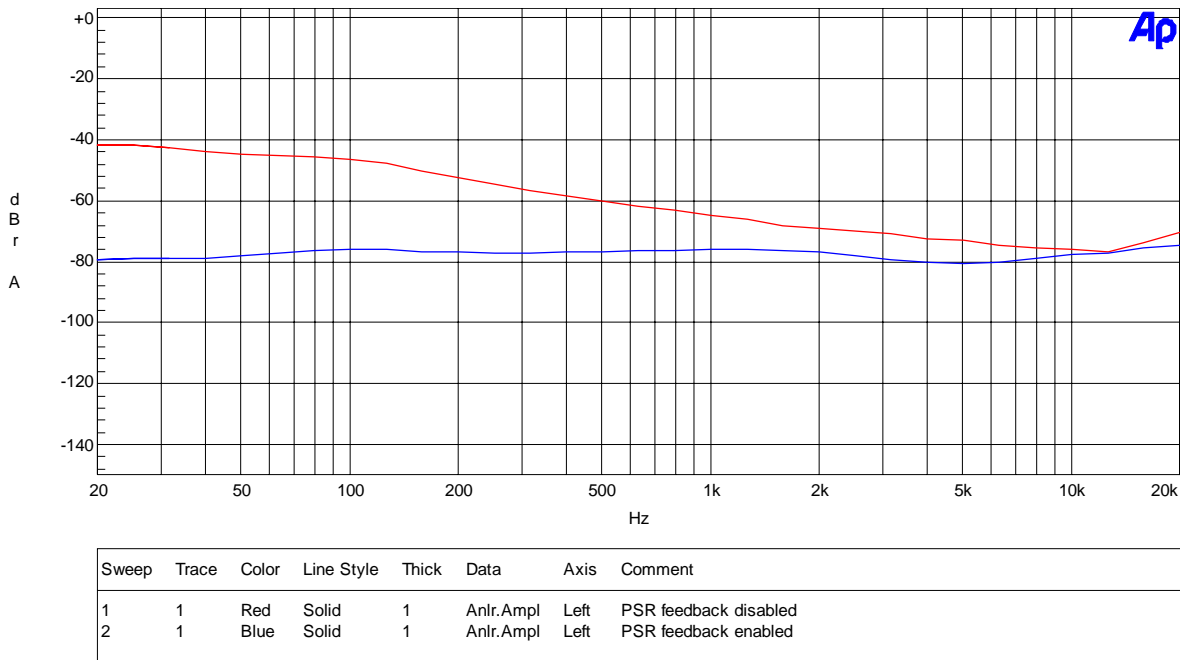


Figure 6. PSR Disabled vs. PSR Enabled

Channel A = "on", but muted (zero data), sweep Channel B frequency @ 0 dBFS

2.3 Power Supply Droop Test

To demonstrate how PSR Feedback can compensate for droop in the power supply rail, perform the following using the CDB44800:

- 1) Using the setup from above, with PSR calibrated and enabled, and Vpower set to +40 V, playback a 1-kHz tone with an amplitude of approximately 10 V peak-to-peak (or any amplitude desired). Use one channel of an oscilloscope to monitor the sine wave output of channel A. Use another channel of the oscilloscope to monitor the DC voltage on Vpower.
- 2) Vary Vpower down to +30 V. Even though the Vpower supply will drop to +30 V from +40 V, the peak-to-peak level of the sine wave output from channel A will remain constant.

This test shows how PSR Feedback will maintain the amplified audio level even if the power supply drops in voltage (common when low-frequency audio is played). The maximum amount of voltage rail droop compensation is limited to 10% of the nominal rail when playing back a full-scale signal. As the signal being played back is reduced in amplitude, more droop in the voltage rail can be compensated.

3. Revision History

Release	Date	Changes
Rev 1	February 2005	Initial Release

Table 1. Revision History

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

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